Table XIV. 3604/3604AL6 Programming Connections.

MODE \ PIN		22 V_{CC2}	24 V_{CC1}
READ	3604	No Connect or +5V	+5V
	3604L-6	+5V	No Connect
PROGRAM	3604	Pulsed 12.5V	Pulsed 12.5V
	3604L-6	Pulsed 12.5V	Pulsed 12.5V
STANDBY POWER	3604L-6	Power dissipation is automatically reduced whenever the 3604L-6 is deselected.	

Programming the 1602A/1702A

In its initial state the 1602A/1702A array will have all outputs low. Programming is accomplished by writing highs in the proper bit locations. The peak I_{DD} current that must be provided for programming the 1602A/1702A is approximately 200 mA, and the entire device can be programmed in about 2 minutes. Figure 38 shows the waveforms required for programming, while Table XV shows the connections used. Table XVI and XVII show the A.C. and D.C. characteristics for programming.

During programming, V_{CC} should be held at ground and V_{BB} should be held at +12V. Address levels are approximately –40V for a logic "0" (output low), and approximately 0V for a logic "1" (output high). Note that these levels are larger in magnitude but in the same polarity sense as those used for reading from the memory:

logic "0": $-1V \leqslant$ logic "0" $\leqslant .65V$,

logic "1": $\geqslant V_{CC} - 2$

where $V_{CC} = 5V \pm 5\%$.

When programming, the negative-going power supplies (V_{DD}) must be pulsed. V_{DD} is pulsed to –47V ±1V. V_{GG} is brought to –35 to –40V, and the complement of the address to be programmed is applied. After the power has been applied for at least 25μS, the address must be returned to its true form 10μS or more after the address has reached its true state, and at least 100 μS after turning on power, the 3 mS program pulse (pin 13) at –47V ±1V may be applied. During the interval when V_{DD} is applied, data signals must be applied to the data output lines. A data level of approximately 0V will result in the location remaining unchanged, while a level of –47V ±1V will program a logic "1" (output high in read mode). After the program pulse is turned off, the V_{DD} and V_{GG} voltages should be

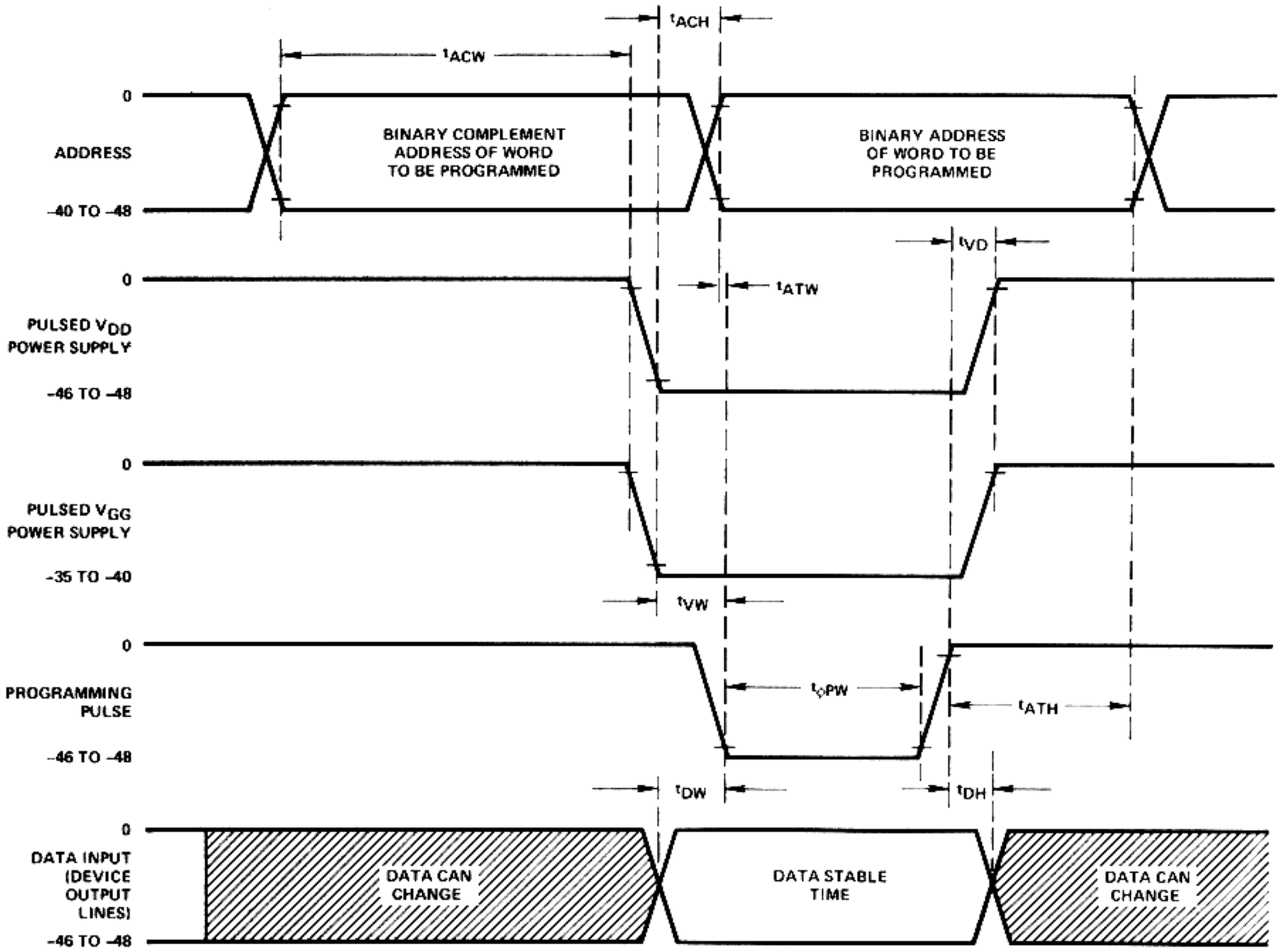

Figure 38. 1602A/1702A Programming Waveforms.

turned off. This turn-off should occur from 10–100μS after removal of the program pulse.

For best results, the 1602A/1702A should be programmed by scanning through the addresses in binary sequence 32 times. Each pass repeats the same series of programming pulses. The duty cycle for applied power must not exceed 20%. As a result, each pass takes about 4 seconds, with the 32 passes taking just over 2 minutes.

ERASING THE 1702A

The 1702A EPROM may be erased by exposure to high intensity, short-wave ultraviolet light at a wavelength of 2537 Angstroms. The recommended integrated dose (i.e., UV intensity X intensity time) is 6W-sec/cm^2. The devices are made with a transparent quartz lid covering the silicon die. Conventional room light, fluorescent light, or sunlight has no measurable effect on stored data, even after years of exposure. However, after 10–20 minutes under a suitable source, the device is erased to a state of all "0's" (outputs low). To prevent damage to the device, it is recommended that no more ultraviolet light exposure be used than that necessary to erase the 1702A.

CAUTION

When using an ultraviolet source of this type, care should be taken not to expose the eyes or skin to the ultraviolet rays, as damage to vision or burns may occur. Also, these short-wave rays may generate considerable amounts of ozone which is potentially hazardous.

Table XV. 1602A/1702A Programming Connections.

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Table XVI. 1602A/1702A D.C. and Operating Characteristics for Programming Operation.

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	$V_{IN} = -48V$
I_{LI2P}	Program and V_{GG} Load Current			10	mA	$V_{IN} = -48V$
I_{BB}	V_{BB} Supply Load Current		10		mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		200		mA	$V_{DD} = V_{prog} = -48V$ $V_{GG} = -35V$
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

2. The V_{BB} supply must be limited to 100mA max current to prevent damage to the device.

Table XVII. 1602A/1702A A.C. Characteristics for Programming Operation.

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle			20	%	
$t_{\phi PW}$	Program Pulse Width			3	ms	$V_{GG} = -35V$, $V_{DD} = V_{prog} = -48V$
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD} , V_{GG} Set Up	100			μs	
t_{VD}	V_{DD} , V_{GG} Hold	10		100	μs	
t_{ACW} [3]	Address Complement Set Up	25			μs	
t_{ACH} [3]	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

Note 3. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.